CLAIMS

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1. A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

switch means disposed on said substrate for selectively interconnecting said inputs to said outputs; and

means disposed on said substrate for controlling said switch means.

2. The invention of Claim 1 wherein said switch means further includes M multiplexers.

3. The invention of Claim 2 wherein each multiplexer is an N to 1 multiplexer and each multiplexer is adapted to receive each of said N electrical inputs.

4. The invention of Claim 3 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable amplifiers.

5. The invention of Claim 4 wherein each multiplexer includes N selection multiplexers.

6. The invention of Claim 5 further including means for summing the outputs of said N selection multiplexers to provide a single output.

7. The invention of Claim 6 further including means for buffering said single output.

8. The invention of Claim 3 wherein each of said N inputs to each of said

multiplexers is received through a respective one of N switchable isolation buffers.

9. The invention of Claim 8 further including means for summing the outputs of said N buffers to provide a single output.

10. The invention of Claim 9 further including means for buffering said single output.

11. The invention of Claim 1 wherein said control means includes a serial in, parallel out shift register.

12. A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

M multiplexers disposed on said substrate for selectively interconnecting said inputs to said outputs, each of said multiplexers being an N to 1 multiplexer, whereby each multiplexer is adapted to receive each of said electrical inputs; and

a serial in, parallel out shift register disposed on said substrate for controlling said multiplexers.

13. The invention of Claim 12 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable amplifiers.

14. The invention of Claim 13 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable isolation buffers.

15. The invention of Claim 14 further including means for summing the outputs of said N buffers to provide a single output.

16. The invention of Claim 15 further including means for buffering said single output.

17. A method for switching including the steps of:

providing a monolithic substrate;

providing a plurality (N) of electrical inputs provided on said substrate;

providing a plurality (M) of electrical outputs provided on said substrate;

providing M, N to 1, multiplexers on said substrate, each multiplexer being adapted to receive each of said electrical inputs, and selectively interconnecting said inputs to said outputs; and

providing a serial in, parallel out shift register on said substrate for controlling said multiplexers.